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(54) Programmable digital delay unit

(57) A programmable digital delay unit (20) presenting a number of cascade-connected delay blocks (22), and a number of controlled bypass elements (23, 24), one for each delay block (22). Each bypass element presents a bypass line (23) and a multiplexer (24) for selectively connecting the input or output of the respective delay block to the input of the next delay block (22). The delay blocks (22) are formed by the cascade connection of flip-flops (28), and the number of flip-flops (28) in each successive delay block (22), from the input of the delay unit (20), decreases in an arithmetic progression to the power of two, so that the selection signals (S_0-S_3) for the respective multiplexers (24) represent the bits of a digital word (M) specifying the required delay.

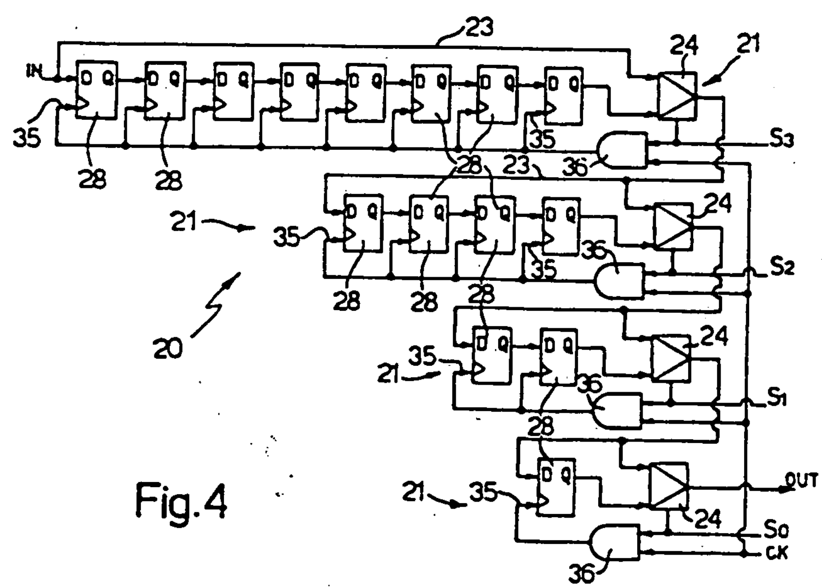

Fig.4

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value of selection signal S_2; the third delay section supplies a delay switchable from two to zero (2-module) depending on the value of S_1; and the fourth (last) delay section supplies a delay switchable from one to zero (1-module) depending on the value of S_0. Therefore, by adding the delays supplied by each section on the basis of the binary values of S_3-S_0, it is possible to obtain a delay ranging between 0 and 15.

In view of the unit delay element sequence in the successive delay sections, selection signals S_0-S_3 present a binary value equal to the corresponding bits of a four-bit digital delay signal; and as in electronic devices the programmable delay required of unit 20 is in fact specified by means of a digital word of this type, delay unit 20 requires no decoding, and the value of the individual bits constituting delay control signal M may be supplied directly to the specific multiplexers.

In the Figure 3 embodiment, unit 20 also comprises a further multiplexer 30 of the same type as 24, i.e. with two data inputs, a selection input and an output. The multiplexer 30 presents one data input connected to the input IN of unit 20 over a general bypass line 31, the other data input connected to the output of the last (fourth) delay section 21, and the selection input connected to the output of a four-input AND gate 32 supplied with the inverse of selection signals S_0-S_3 The output OUT of multiplexer 30 also constitutes the output of unit 20 so that, when no delay is required and selection signals S_0-S_3 all present a low logic value, input signal IN may be supplied directly to the output via general bypass line 31 and multiplexer 30, without going through multiplexers 24 of all the delay sections 21, thus eliminating any possibility of undesired delays.

The minimum configuration of unit 20, i.e. without multiplexer 30 and AND gate 32, comprises fifteen unit delay elements (flip-flops) 28 and four multiplexers 24. In general, a delay unit for supplying a programmable delay of 0 to 2^n-1 specified by an n-bit digital signal requires 2^n-1 flip-flops and n multiplexers. Since, as stated, the structure requires no decoding of the delay control signal, it can be implemented with a small number of only two types of components (flip-flops and multiplexers), or three types in the case of the complete solution shown in Figure 3. In view of the simple nature of the individual components involved, unit 20 is therefore easily implementable in a very small area, particularly for VLSI applications.

Another important advantage of the structure described is that it presents a maximum fanout of 2, in that each multiplexer drives only two components (the first flip-flop and the multiplexer of the next delay section) and each flip-flop drives only one component, thus permitting the use of extremely high operating frequencies.

If a reduction in power consumption is required for delays below the maximum programmable value, the Figure 3 structure may be further improved by providing the possibility of turning off the flip-flops of individual delay blocks 22 when bypassed by respective line 23.

Such a solution is shown in Figure 4 which is similar to Figure 3 and in which components 30-32 are omitted and unit delay elements 28 are shown in more detail in the form of D type flip-flops with a clock input 35. As shown in Figure 4, in which the components are indicated using the same numbering system as in Figure 3, the clock inputs 35 of flip-flops 28 of each delay section 21 are connected to one another and to the output of a respective two-input AND gate 36 supplied with the respective selection bit S_0-S_3 and with clock signal CK.

As such, when selection signal S_i of a specific delay section 21 presents a low logic value, by connecting the respective bypass line 23 to its output and disconnecting the output of the respective delay block, the respective AND gate 36 prevents the clock strokes from reaching the flip-flops of the delay block and in practice disables them, thus reducing consumption, on average, by half at the expense of a slight increase in complexity and area for the addition of n AND gates.

Figures 5 to 7 show further, hybrid, embodiments of the invention, wherein the potential afforded by delay blocks in decreasing numbers, as in Figures 3 and 4, is not exploited fully.

More specifically, Figure 5 shows a delay unit 40 comprising an 8-module delay section 41 (i.e. with a delay block formed by the cascade connection of eight unit delay elements 28) followed by a delay section 42 programmable from 0 to 7. Programmable delay section 42 comprises seven delay elements 28 and seven multiplexers 24, each multiplexer 24 presenting two data inputs connected respectively to the output of a preceding unit delay element 28 and to the output of the multiplexer 24 of section 41, and an output connected to the input of the next unit delay element 28. Multiplexers 24 of sections 41, 42 receive selection signals S_0-S_7 which no longer correspond to the bits of a digital delay control signal, as in the case of signal M in Figures 1-3, so that decoding logic (not shown) is required at least as regards signals S_0-S_6 (signal S_7 corresponds to the most significant bit of digital delay control signal M).

This solution presents a maximum fanout of 8 (the number of loads driven by the output multiplexer 24 of section 40) and requires 8 multiplexers.

Alternatively, embodiment 40 in Figure 5 may be modified by replacing section 41 with the cascade connection of seven 1-module sections (i.e. comprising one unit delay element 28), wherein the multiplexers 24 of each 1-module section receive at the two data inputs the output of flip-flop 28 in its own section and the output of the multiplexer 24 of the preceding section. This provides for reducing fanout to a maximum of two and for increasing operating frequency for a given number of components.

Figure 6 shows a delay unit 44 featuring three 4-module delay sections 45 (with four unit delay elements 28) and a delay section 46 programmable from 0 to 3 and presenting three unit delay elements 28 and three multiplexers 24 connected as described with reference to Figure 5. In this case also, the multiplexers 24 of sec-

erating enabling signals supplied to said clock inputs of said unit delay elements (28).

13. A delay unit as claimed in one of the foregoing Claims, characterized in that said unit delay elements are flip-flops (28).

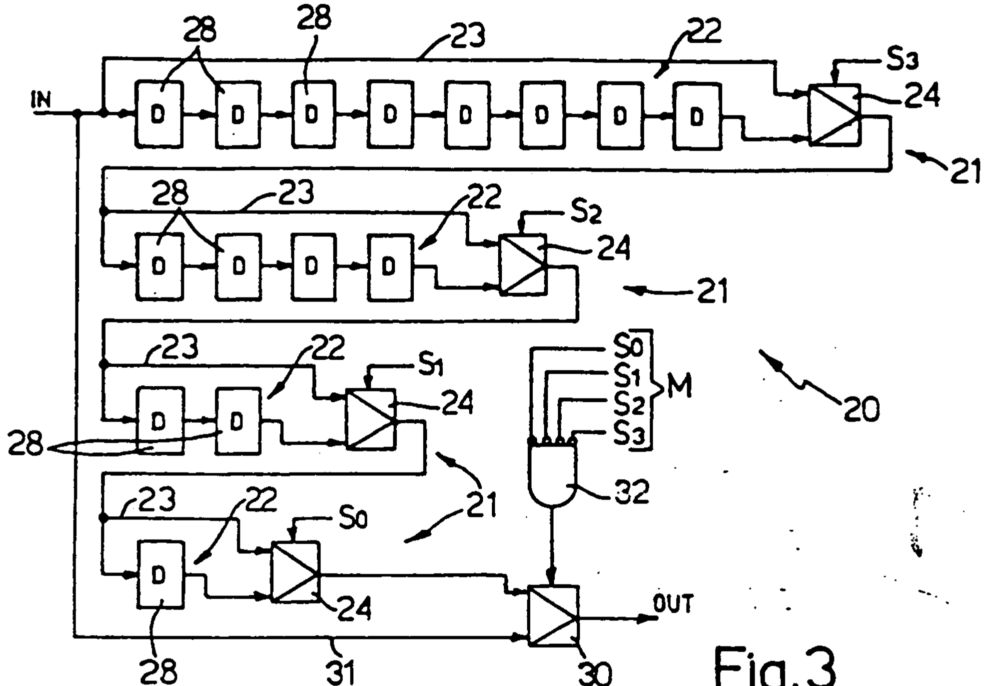
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Fig.3

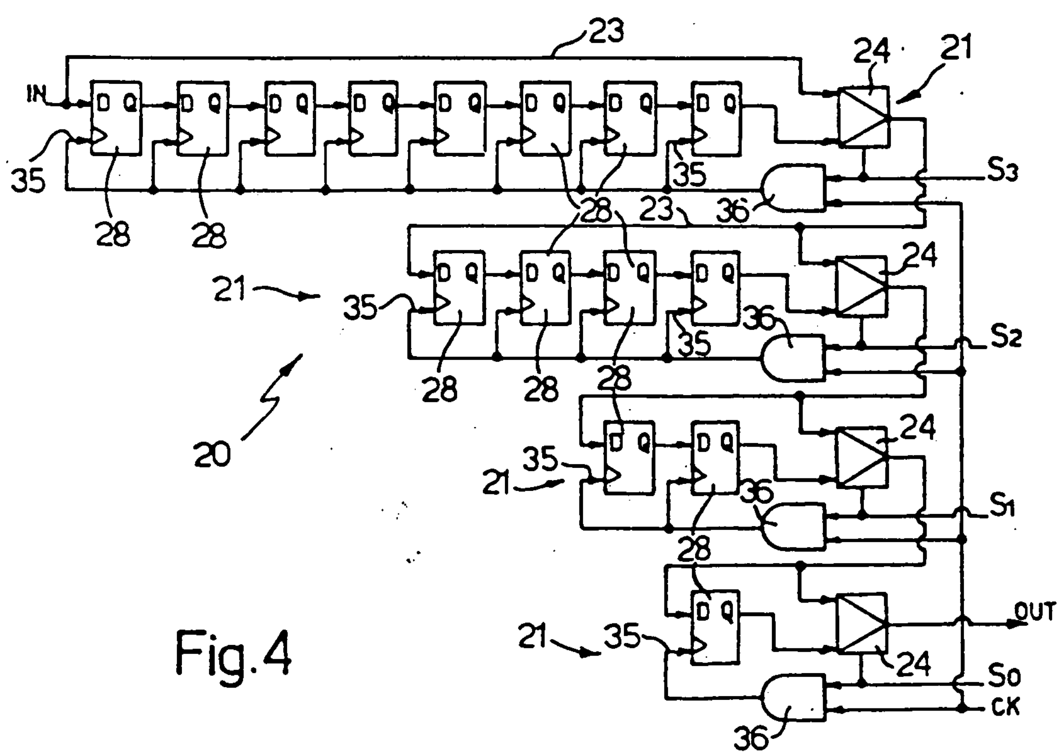
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Fig.4

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 83 0445

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US-A-5 204 559 (DEYHIMY IRA ET AL) 20 April 1993 * the whole document *	1-10	H03K5/13
X	EP-A-0 446 891 (MITA INDUSTRIAL CO LTD) 18 September 1991 * page 3, line 39 - page 6, line 47; figure 2 *	1-12	
X	US-A-4 939 677 (OTUJI TAIICHI ET AL) 3 July 1990 * figures 1,3-5 *	1-10	
X	EP-A-0 361 806 (ADVANCED MICRO DEVICES INC) 4 April 1990 * the whole document *	1-12	
A	EP-A-0 208 049 (ADVANTEST CORP) 14 January 1987 * figure 5 *	1-12	TECHNICAL FIELDS SEARCHED (Int.Cl.6)
A	DE-A-41 10 340 (TEKTRONIX INC) 17 October 1991		H03K

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	6 March 1995	Segaert, P

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